What is claimed is:

1. A data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes are fetched;

a fetch address operation circuit which calculates a fetch address used to fetch an instruction code in the instruction queue;

a fetch circuit which fetches an instruction code that is read out based on the fetch address into the instruction queue; and

a branch information setting circuit which decodes a branch setting instruction instructing a branch to a branch target address when the fetch address is a branch address, stores the branch address in a branch address storage register, and stores the branch target address in a branch target address storage register,

wherein the fetch address operation circuit includes a circuit which compares one of a previous fetch address and an expected next fetch address with a value stored in the branch address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result.

2. A data processing device using pipeline control, comprising:

an instruction queue in which a plurality of instruction codes are fetched;

a fetch address operation circuit which calculates a fetch address used to fetch an instruction code in the instruction queue;

a fetch circuit which fetches an instruction code that is read out based on the fetch address into the instruction queue; and

a branch information setting circuit which decodes a branch setting instruction instructing a branch to a branch target address when the fetch address is a branch address, stores the branch address in a branch address storage register, and stores the

branch target address in a branch target address storage register,

wherein the fetch address operation circuit includes a circuit which compares an expected next fetch address obtained by incrementing a value in a fetch program counter by one instruction length with a value stored in the branch address storage register, and then outputs a value stored in the branch target address storage register as a next fetch address when the expected next fetch address coincides with the value in the branch address storage register, or outputs the expected next fetch address as a next fetch address when the expected next fetch address does not coincide with the value in the branch address storage register.

3. The data processing device as defined in claim 1, wherein:

the branch setting instruction includes a loop instruction which designates a loop count;

the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop count, and stores the loop count designated by the loop instruction; and

the fetch address operation circuit includes a circuit which outputs a value stored in the branch target address storage register as a next fetch address until the number of times the branch to the branch target address repeats reaches the loop count.

4. The data processing device as defined in claim 2, wherein:

the branch setting instruction includes a loop instruction which designates a loop count;

the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop count, and stores the loop count designated by the loop instruction; and

the fetch address operation circuit includes a circuit which outputs a value

stored in the branch target address storage register as a next fetch address until the number of times the branch to the branch target address repeats reaches the loop count.

5. The data processing device as defined in claim 1, wherein:

the branch setting instruction includes a loop instruction which designates a loop count;

the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop count, and stores the loop count designated by the loop instruction; and

the fetch address operation circuit includes a circuit which decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value obtained by incrementing the branch address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

6. The data processing device as defined in claim 2, wherein:

the branch setting instruction includes a loop instruction which designates a loop count;

the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop count, and stores the loop count designated by the loop instruction; and

the fetch address operation circuit includes a circuit which decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value obtained by incrementing the branch address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

7. The data processing device as defined in claim 3, wherein:

the branch setting instruction includes a loop instruction which designates a

loop count;

the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop count, and stores the loop count designated by the loop instruction; and

the fetch address operation circuit includes a circuit which decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value obtained by incrementing the branch address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

8. The data processing device as defined in claim 4, wherein:

the branch setting instruction includes a loop instruction which designates a loop count;

the branch information setting circuit decodes the loop instruction which instructs to repeat a branch to the branch target address the number of times equal to the loop count, and stores the loop count designated by the loop instruction; and

the fetch address operation circuit includes a circuit which decrements a value set in the loop counter each time when a branch to the branch target address occurs, and outputs a value obtained by incrementing the branch address by one instruction length as a next fetch address when the value of the loop counter reaches zero.

9. The data processing device as defined in claim 3, wherein:

the loop instruction has the branch target address which is fixed relative to the loop instruction and also has no branch target address information in an operand; and

the branch information setting circuit includes a circuit which calculates the value fixed relative to the loop instruction and stores the calculated value in the branch target address storage register.

10. The data processing device as defined in claim 4, wherein:

the loop instruction has the branch target address which is fixed relative to the loop instruction and also has no branch target address information in an operand; and

the branch information setting circuit includes a circuit which calculates the value fixed relative to the loop instruction and stores the calculated value in the branch target address storage register.

11. The data processing device as defined in claim 5, wherein:

the loop instruction has the branch target address which is fixed relative to the loop instruction and also has no branch target address information in an operand; and

the branch information setting circuit includes a circuit which calculates the value fixed relative to the loop instruction and stores the calculated value in the branch target address storage register.

12. The data processing device as defined in claim 6, wherein:

the loop instruction has the branch target address which is fixed relative to the loop instruction and also has no branch target address information in an operand; and

the branch information setting circuit includes a circuit which calculates the value fixed relative to the loop instruction and stores the calculated value in the branch target address storage register.

13. Electronic equipment comprising:

the data processing device as defined in claim 1;

means for receiving input data; and

means for outputting a result of processing the input data by the data processing device.

14. Electronic equipment comprising:

the data processing device as defined in claim 2;

means for receiving input data; and

means for outputting a result of processing the input data by the data processing device.

15. Electronic equipment comprising:

the data processing device as defined in claim 3;

means for receiving input data; and

means for outputting a result of processing the input data by the data processing device.

16. Electronic equipment comprising:

the data processing device as defined in claim 4;

means for receiving input data; and

means for outputting a result of processing the input data by the data processing device.

17. Electronic equipment comprising:

the data processing device as defined in claim 5;

means for receiving input data; and

means for outputting a result of processing the input data by the data processing device.

18. Electronic equipment comprising:

the data processing device as defined in claim 6;

means for receiving input data; and

means for outputting a result of processing the input data by the data processing device.